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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,432	03/07/2002	Shigetaka Asano	1076.1073	8832

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/091,432	ASANO, SHIGETAKA	
	Examiner	Art Unit	
	Qutub Ghulamali	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-23* is/are allowed.

6)☒ Claim(s) *1,2,4-8 and 12-14* is/are rejected.

7)☒ Claim(s) *3, 9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Remarks/Amendments filed by the applicant on 11/07/2006.

2. Amendment to claims 2-5, 9, 11 and 18, is hereby acknowledged. The amendment is considered acceptable and therefore, the objection of claims 2-5, 9, 11 and 18, has been withdrawn.

Response to Remarks/Arguments

3. Applicant's remarks/arguments, see pages 8-9, filed 11/07/2006, regarding claims 1, 2, 4-7 and 14 have been fully considered but are not persuasive.

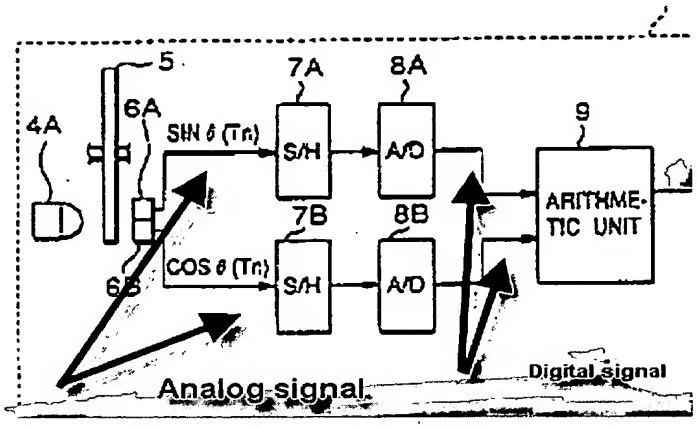
4. The applicant alleges that Tsutsumishita in combination with Kashida does not teach or suggest "delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal in a second path that is different from the first path".

The examiner response – The examiner disagrees and respectfully would like to draw applicant's attention to Tsutsumishita, wherein Tsutsumishita discloses an analog control method comprising:

converting the analog signal to a digital signal via a first path (figs. 1, 2, 4; col. 12, lines 22-31);

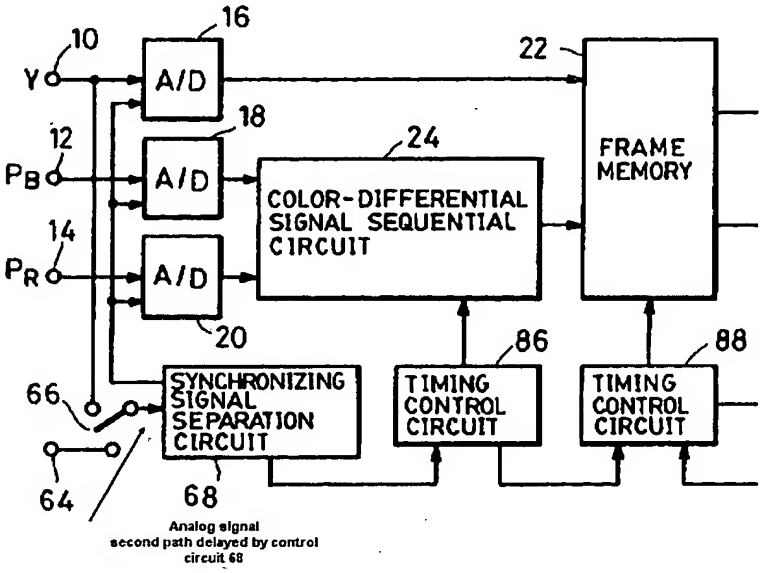
performing an arithmetic processing of the digital signal via the first path to generate a control signal for controlling the analog signal (col. 7, lines 1-28; col. 12, lines 22-26). The Tsutsumishita reference however, does not explicitly disclose a second path with a delay for delaying the analog signal.

Fig. 4



What Tsutsumishita does not explicitly disclose is delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal in a second path that is different from the first path. This feature is satisfied by Kashida, as Kashida discloses a second path with a delay element (timing control with delay, element 86) delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal in a second path that is different from the first path (the A/D path) (col. 5, lines 7-24; col. 6, lines 39-46) and controlling the delayed analog signal in accordance with the control signal in the second path. It would have been obvious to a person of ordinary

skill in the art at the time the invention was made to use a delay circuit to delay analog signal in a second path in the analog control circuit with control as taught by Kashida in the circuit of Tsutsumishita because by providing the delay that is equivalent to the ADC latency can mitigate time differences in the analog signal processing corresponding to the latency of the ADCs.



Based on the information disclosed in the combined arts of Tsutsumishita and Kashida, the examiner believes that the claimed limitations recited in claims 1, 6, 7 and 14, are satisfied to the extent provided with the explanation above. The claim rejection is, therefore, maintained.

As per applicant's remarks, with reference to dependent claims 2, 4, 5, 8, 12 and 13, the rejection of these claims are based on the base claim they represent and therefore, they are likewise rejected. The examiner also points out that the suggestion to combine may

be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved. See id. at 1357, 47 USPQ 2d at 1458. Moreover, as long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor. See In re Dillon, 919 F .2d 688, 693, 16 USPQ 2d 1897, 1901 (Fed. Cir. 1990) (en banc), cert. Denied, 500 U.S. 904 (1991) and In re Beattie, 974 F .2d 1309, 1312, 24 USPQ 2d 1040, 1042 (Fed. Cir. 1992).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4-7, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumishita (USP 5,721,546) in view of Kashida et al (USP 5,400,148).

Regarding claims 1, 6, Tsutsumishita discloses an analog control method comprising:

converting the analog signal to a digital signal via a first path (figs. 1, 2, 4; col. 12, lines 22-31);

performing an arithmetic processing of the digital signal via the first path to generate a control signal for controlling the analog signal (col. 7, lines 1-28; col. 12, lines 22-26).

The Tsutsumishita reference however, does not explicitly disclose a second path with a delay for delaying the analog signal. Kashida however, discloses a second path with a delay element (timing control with delay, element 86) delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal in a second path that is different from the first path (the A/D path) (col. 5, lines 7-24; col. 6, lines 39-46) and controlling the delayed analog signal in accordance with the control signal in the second path. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a delay circuit to delay analog signal in a second path in the analog control circuit with control as taught by Kashida in the circuit of Tsutsumishita because by providing the delay that is equivalent to the ADC latency can mitigate time differences in the analog signal processing corresponding to the latency of the ADCs.

As per claim 2, Tsutsumishita discloses:

sampling the analog signal at a predetermined timing to generate a sampling value (the A/D circuit by design converts the analog signal in discrete steps taken as predetermined time values of analog signal to produce a sample value) (figs. 1, 2, 4; 26, 28; col. 12, lines 22-31, 40-51);

generates control signal (predicted position data) in accordance with the sampling value (col. 7, lines 1-28; col. 12, lines 22-26); and inherent to the analog to digital conversion is the delay, in sampling the signal having a sampling value correspond to the predetermined sampling time taken in discrete steps (figs. 1, 2, 4; 26, 28; col. 12, lines 22-31, 40-51).

As per claims 4 and 5, Tsutsumishita discloses:

sampling the analog signal at a plurality of predetermined timing to generate a plurality of sampling values (the ADC circuit by design converts the analog signal in discrete steps taken as predetermined time values of analog signal to produce a sample value) (figs. 1, 2, 4; 6, 26, 28; col. 8, lines 39-52; col. 12, lines 22-31, 40-51);

calculating the plurality of sampling values to generate control signal (predicted position data) in accordance with the sampling value (col. 7, lines 1-28; col. 12, lines 22-26); and inherent to the analog to digital conversion is the delay, in sampling the signal having a sampling value correspond to an arbitrary sampling time or at a timing previous to each sampling taken in discrete steps to reproduce analog signal in quantized steps (figs. 1, 2, 4; 26, 28; col. 12, lines 22-31, 40-51).

As per claim 7, Tsutsumishita discloses an analog signal control comprising:

An analog-to-digital (ADC) signal conversion, the ADC (element 8A, 8B) located in the first path and converting an analog signal to generate a digital signal (figs. 1, 2, 4; col. 12, lines 22-31);

A digital arithmetic circuit (element 9) located in the first path and connected to the ADC for performing an arithmetic processing of the digital signal to generate a control signal for controlling the analog signal (col. 7, lines 1-28; col. 12, lines 22-26). The Tsutsumishita reference however, does not explicitly disclose a delay circuit located in a second path that is different from the first path, and delaying the analog signal

corresponding to a latency caused by the ADC and the digital arithmetic circuit to generate a delayed analog signal, and

an analog control circuit, located in the second path.

Kashida, however, discloses a second path with a delay element (timing control with delay, element 86) delaying the analog signal corresponding to a latency caused by the ADC and the digital arithmetic circuit to generate a delayed analog signal and an analog control circuit connected to the digital arithmetic unit and delay for controlling the delayed analog input signal (col. 5, lines 7-24; col. 6, lines 39-46). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a delay circuit to delay analog signal in a second path in the analog control circuit with control as taught by Kashida in the circuit of Tsutsumishita because by providing the delay that is equivalent to the ADC latency can mitigate time differences in the analog signal processing corresponding to the latency of the ADCs.

Regarding claim 14, Tsutsumishita discloses an automatic gain control comprising:

A first control loop located in a path for receiving an analog signal to generate a control signal for setting a predetermined gain for use in amplifying the analog signal (figs. 1, 2, 4; col. 12, lines 22-31). Tsutsumishita is silent regarding:

a delay circuit located in a path that is different from the first path for receiving the analog signal and delaying an analog signal corresponding to a latency caused by the first loop to generate a delayed a delayed analog signal; and a gain control amplifier

located in the second path and connected to the delay circuit and the first loop for amplifying the delayed analog signal in accordance with a predetermined gain set by the control signal to generate an amplified analog signal. Kashida discloses a delay circuit (timing control with delay, element 86) located in a path that is different from the first path for receiving the analog signal and delaying an analog signal corresponding to a latency caused by the first loop to generate a delayed a delayed analog signal; and a gain control amplifier (elements 30, 32 with 31, 33) located in the second path and connected to the delay circuit and the first loop for amplifying the delayed analog signal in accordance with a predetermined gain set by the control signal to generate an amplified analog signal (col. 1, lines 37-50, 51-60). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a delay circuit to delay analog signal in a second path in the analog control circuit with control and gain control amplifier as taught by Kashida in the circuit of Tsutsumishita because by providing the delay that is equivalent to the ADC latency can mitigate time differences in the analog signal processing corresponding to the latency of the ADCs.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumishita (USP 5,721,546) in view of Oishi et al (US Patent 6,563,859).

Regarding claim 8, Tsutsumishita discloses an analog signal controller wherein: the analog signal controller operates in accordance with a clock signal (col. 1, lines 30-35; col. 2, lines 15-44). Tsutsumishita however is silent regarding "the delay circuit includes a pair of switches which operate complementary to each other in synchronism

with the clock signal, and delays the analog signal by switching the pair of switches". Oishi in a similar field of endeavor discloses a plurality of delay switches (fig. 12501-1 to 501-N), which operate complementary to each other in synchronism with the clock signal, and delays the analog signal by switching the plurality of switches (col. 11, lines 18-34). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use delay switches to delay analog signals (sampling period of the A/D converters) in synchronism with the clock signal as taught by Oishi in the circuit of Tsutsumishita because it can provide equalization in frequency shift of the received signal to be extracted.

8. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumishita (USP 5,721,546) in view of Gurvich (US Patent 6,897,724).

Regarding claims 12 and 13, Tsutsumishita discloses all of the claim limitations but is silent regarding a delay circuit includes a capacitor having a capacitance (variable) value for delaying the analog signal corresponding to latency (delay, error). Gurvich in a similar field of endeavor shows a system wherein capacitors are used in the delay circuit for delaying the signal, shows the capacitor could be a variable capacitor such as a varactor (variable capacitor) (col. 5, lines 25-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use fixed or variable capacitors at the switch nodes as taught by Gurvich in the circuit of Tsutsumishita because it can allow proper group delay adjustments with the transmission of signal in the transmission line.

Allowable Subject Matter

9. Claims 15-23 allowed.

10. Claims 3 and 9-11, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and any claim objections noted above.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday, 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QG.
January 11, 2007.

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER